REMARKS

Claims 75-84 have been added. Claims 1-7 and 51-84 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

The Abstract has been amended to place the Abstract into conformance with present PTO rules. No new matter is added by the amendment to the Abstract.

Claims 1-7 and 51-73 stand rejected under 35 U.S.C. §102(e) as being anticipated by Forbes, U.S. Patent No. 5,897,351. The Examiner also asserts (p. 11, item 4) that "Claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over Forbes, U.S. Patent No. 5,897,351." Applicant infers that the Examiner had intended to reject claims 52, 53 and 74. Clarification of the rejection is again requested.

Anticipation is a legal term of art. In order to present a valid finding of anticipation, a number of different legal standards must be simultaneously satisfied: (i) the reference must include every element of the claim within the four corners of the reference (see MPEP §2121); (ii) the elements must be set forth as they are recited in the claim; (iii) the teachings of the reference cannot be modified (see MPEP §706.02, stating that "No question of obviousness is present" in conjunction with anticipation); and (iv) the reference must enable the invention as recited in the claim (see MPEP §2121.01).

The §102 rejection of claims 1-7 and 51-73 is believed to be in error. Specifically, the PTO and Federal Circuit provide that §102 anticipation

requires that each and every element of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of any claimed element negates the anticipation. *Kloster Speedsteel AB, et al. v. Crucible, Inc., et al.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).

To further delineate and clarify the legal meaning of the term "anticipation", Applicant notes the requirements of MPEP §2131, which states that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM." This MPEP section further states that "'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

Additionally, the reference must enable the claimed invention. This is explained in MPEP §2121.01, entitled "Use of Prior Art in Rejections Where Operability Is In Question". This MPEP section states that "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated

test is whether a reference contains an 'enabling disclosure'... ." *In re Hoeksema*, 399 F.2d 269, 158 USPQ 596 (CCPA 1968). A reference contains an "enabling disclosure" if the public was in possession of the claimed invention before the date of invention. Forbes '351 does not and cannot enable the invention as recited in the claims because Forbes '351 does not describe it.

The Examiner states (p. 2) that Forbes '351 teaches "forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas, with some widths being no greater than 1 um, at least two of the widths being different (Fig.3 and Col.7, lines: 55-63)." The Examiner is mistaken.

As used with respect to the electrical arts, "shallow trench isolation" is a conventional term of art with a well-defined meaning. This term refers to more than simply "a shallow trench isolating one feature from another." The term refers to a specific process employed in silicon device technology which involves:

i) masking;

ii) anisotropic etching to provide a steep-sided, sharp-cornered trench between features to be isolated from one another;

iii) a short thermal oxidation process to provide a Si-SiO_2 interface having controlled electronic properties;

iv) an oxide deposition process, typically by thermal decomposition of tetraethylorthosilicate (TEOS), which process not only fills the trench with deposited SiO_2 but also coats the entire substrate with deposited SiO_2; and

v) chemical-mechanical polishing to remove excess deposited SiO_2 from regions where it is not desired.

The result of such a process is obviously a planar surface that, in turn, facilitates further processing. Such is illustrated, for example, in Applicant's Fig. 2 and is exemplified in the subsequent Figs. The benefits of such processing, compared to prior art LOCOS processes, include higher spatial resolution and increased planarity. As a result, and as noted by Wolf (Silicon Processing for the VLSI Era, 2ND Ed., Lattice Press, Sunset Beach, CA, copyright 2000, p. 301), STI is the most popular isolation technology for advanced devices having linewidths of 0.25 micrometer or less.

Objective evidence for the meaning of this term of art can be found in a number of ways. For example, a search based on the term "shallow trench isolation" for the years 1991-1995 yields a total of 60 references that include this term. A search based on this term for the years 1996-present provides a total of 2728 references using this term, with increasing frequency in more recent years, as is summarized below in Table I.

Table I. Relative frequency of STI in USPTO database.

Year	Number of patent references
1991-95	60
1996	20
1997	38
1998	120
1999	349
2000	637
2001	898
2002	666 (Jan.-Sept.)
1996-2002	2728

Several examples of patents issued prior to filing of the present application are enclosed that describe shallow trench isolation technology. For example, U.S. Patent No. 5,447,884, entitled "Shallow Trench Isolation With Thin Nitride Liner", issued to Fahey et al., describes (col. 1, line 54 through col. 2, line 38) steps (i) through (iv) above. U.S. Patent No. 5,851,900, entitled "Method Of Manufacturing A Shallow Trench Isolation For A Semiconductor Device" describes (Fig. 8 and associated text) step (v), in addition to describing steps (i) through (iv).

A summary of STI processes (Wolf, Silicon Processing for the VLSI Era, 2ND Ed., Lattice Press, Sunset Beach, CA, copyright 2000, pages 300, 301 and 830-832) is enclosed to illustrate that "shallow trench isolation" is a term of art referring to a specific type of process. From this evidence and the figures presented in Table I, one can deduce that "shallow trench isolation" is a term of art describing a specific type of isolation process that has come into wide usage during the last several years and does not merely reflect the depth of isolation trenches employed in MOS device technology.

This type of process is distinct from the processes taught by Forbes '351. In particular, LOCOS is distinct from STI and is not arbitrarily interchangeable with STI.

The Examiner refers to Fig. 3 and col. 7, lines 55-63. This passage describes a LOCOS process.

> Active areas which define the silicon island-like active areas 300 are then defined on the individual silicon bars 404, using a standard process, such as LOCal Oxidation of Silicon (**LOCOS**), as shown in FIG. 4F, to form oxide 416 between the active areas 300. Depending on the width of the silicon bars 404, the area of

> these active areas 300 is approximately one square micron or less for sub-micron technology and approximately 0.0625 square microns or less for sub-0.25 micron technology.

This is clearly and plainly a reference to a LOCOS isolation process. It does not teach or disclose a shallow trench isolation process. As noted above, LOCOS and STI are different processes, used to provide different results, and are NOT arbitrarily interchangeable.

The terms "LOCOS" and "shallow trench isolation" are terms of art having specific and different meanings to those of ordinary skill in the semiconductor arts. Copies of pp. 330-1 and 367-8, taken from S. Wolf, "Silicon Processing for the VLSI Era", copyright 1995, Lattice Press, Sunset Beach, CA, describing these two, different technologies, have been previously provided for the Examiner's convenience. Note in particular that the text on p. 367 contrasts these two technologies and further shows why these two technologies are not arbitrarily interchangeable. The definition of the term "shallow trench isolation" provided in Wolf also makes clear that the methods for isolation of silicon islands taught by Forbes '351 are not arbitrarily interchangeable with shallow trench isolation as recited in all of Applicant's independent claims.

The Examiner states (p. 4) that "Examiner has reviewed the entire Forbes reference and cannot find where LOCOS is used to isolate the active region." Forbes '351 teaches (col. 5, lines 3-6) that "An oxide layer 302 isolates the major portion of the silicon island 300 from the main body portion of the underlying substrate 301 as will be shown."

Forbes '351 teaches methods described at col. 6, line 30 through col. 8, line 37 to form silicon bars 404. Forbes '351 also teaches that these may be formed using processes as described at col. 6, lines 47-62. These techniques are not shallow trench isolation, and Forbes '351 certainly does not represent them as such.

Forbes '351 teaches (col. 6, line 59 et seq.) formation of Si_3N_4 caps 406. Such caps are employed in LOCOS processes because they are relatively impermeable to penetration by oxygen during oxidation of the substrate. Thus, **LOC**al **O**xidation of **S**ilicon can be carried out in a controlled fashion as desired.

Forbes '351 then teaches (col. 7, line 21 et seq.) that the isolation oxide 302 is formed by "a wet, oxidizing ambient". Such comprises local oxidation of silicon to form silicon oxide for isolating areas of a silicon substrate from one another. Such does not comprise deposition of oxide as is part of an STI process as recognized in the relevant arts.

Forbes '351 does not teach shallow trench isolation. In fact, Forbes '351 is void of the word "shallow". In other words, the term "shallow" does not appear anywhere in Forbes '351.

Applicant will attempt to lay this out for the Examiner in a nutshell.

1) Forbes '351 teaches use of LOCOS techniques.

2) Forbes '351 is being cited as anticipating Applicant's claims.

3) Applicant's claims do not recite LOCOS.

4) Applicant's claims recite STI.

5) Forbes '351 does not teach or disclose STI.

6) Anticipation requires that the reference teach or disclose the claimed subject matter.

7) Therefore, Forbes '351 does not anticipate the invention as recited in any of Applicant's claims.

8) As a result, the anticipation rejections are in error and should be withdrawn, and Applicant's claims 1-7 and 51-73 should be allowed.

It is inappropriate to modify the teachings of a reference in attempting to make a valid anticipation rejection under 35 U.S.C. §102. This is explained more fully in MPEP §706.02.

In a subsection entitled "DISTINCTION BETWEEN 35 U.S.C. 102 AND 103", this MPEP section states that: "The distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present." In other words, no modification or inference is allowed in a determination of anticipation. Put another way, the identical invention must be described and enabled within the four corners of the reference to provide a valid finding of anticipation.

Forbes '351 simply does not describe the invention as recited in any of Applicant's claims. It is not appropriate to modify the teachings of Forbes '351 to try to find anticipation.

The Examiner states (p. 5) that "FORBES DOES TEACH shallow trench isolation", apparently based on the ordinary meanings of the terms "shallow", "trench" and "isolation". However, as used in the electrical arts, the term of art "shallow trench isolation" does not simply mean "a shallow trench that

isolates". It refers to a much more specific process, and Applicant has provided credible, objective evidence to this effect.

Labeling the technique taught by Forbes '351 "shallow trench isolation" or substituting the silicon bar structures 404 taught by Forbes '351 for the shallow trench isolation structures recited in all of Applicant's independent claims gives the term of art "shallow trench isolation" a meaning repugnant to the ordinary meaning of the term as used in the art and as evidenced by Wolf, USPTO patent cites and the enclosed exemplary patents.

Applicant notes the requirements of MPEP §608.01(o), entitled "Basis for Claim Terminology in Description". This MPEP section states that "The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import; and in mechanical cases, it should be identified in the descriptive portion of the specification by reference to the drawing, designating the part or parts therein to which the term applies. A term used in the claims may be given a special meaning in the description. No term may be given a meaning repugnant to the usual meaning of the term."

The Examiner's arbitrary conflation of terms of art, specifically the local oxidation of silicon taught by Forbes '351 and the shallow trench isolation recited in Applicant's claims, gives both of these terms meanings repugnant to the usual meanings of these terms as used by those of ordinary skill in the art. Such is improper and should be retracted.

The Examiner makes a series of statements (p. 5) to the effect that Forbes '351 teaches trench isolation, and attempts to re-characterize a

number of statements made by the Examiner and Applicant. Forbes '351 does indeed teach trench isolation. Forbes '351 does not teach "shallow trench isolation", and Forbes '351 makes no such representation.

The Examiner states (p. 6) that "Forbes teaches the exact same process of forming and refilling the trenches with an oxide - Col.7, lines:48-56 describes refilling the shallow trenches." The Examiner is again mistaken.

Applicant reproduces that text below, along with the text immediately preceding it (col. 7, lines 20-56):

> The substrate 301 is oxidized using a standard silicon processing furnace at a temperature of approximately 900 to 1,100 degrees Celsius, followed by stripping of the Si_3N_4 cap 406, producing the structure shown in FIGS. 4D and 4E. A wet, oxidizing ambient is used in the furnace chamber to oxidize the exposed silicon regions on the lower part of the trenches 402 in a parallel direction to the surface of the substrate 301. The substrate 301 is oxidized for a time period, such that oxide 302 partially undercuts the bottom of the silicon bars 404, producing first portions of the silicon bars from which the island-like active areas 300 of silicon material will be defined in a subsequent process step, which are partially isolated from the substrate by the layer of oxide 302, and second portions of the silicon bars that define the pedestals 304 which support the silicon islands 300 that will be formed and which remain in contact with the substrate. In contrast to the process disclosed in the referenced patent application, in the process according to the present invention, the island-like active areas of silicon subsequently produced are not completely isolated from the substrate 301 by oxidation. A portion of the pedestal 304 is maintained to contact the body of the n-channel transistor 28 and a portion 304a of the pedestal is maintained to be in contact with the drain region 49 of the p-channel transistor 26 that is formed in a subsequent process step, the pedestal portion 304a being shown in FIG. 3 in contact with the drain region 49.
>
> The larger volume of oxide substantially fills the trenches 402 between the silicon bars 404. The time period for oxidation depends on the width of the silicon bars 404 and the effective width after the undercut step. For example, for sub-micron technology, oxidation time is approximately three to four hours.

For sub-0.25 micron technology, oxidation time is approximately one hour.

Forbes '351 is using a Si_3N_4 cap to **LOC**ally **O**xidize **S**ilicon to provide oxide 302, albeit in a different form than is typical of LOCOS. As with conventional LOCOS, the Si_3N_4 cap prevents some silicon from reacting with oxygen, while exposed silicon is locally oxidized. Forbes '351 is not teaching STI in the conventional sense of the term as it is used by those of skill in the relevant arts. In other words, the resemblance that the Examiner is noticing to STI in the teachings of Forbes '351 is superficial and is apparently based on a misunderstanding of the meaning of the term "shallow trench isolation" as it is used by those of ordinary skill in the relevant arts.

Applicant has provided the Examiner with technical information describing both techniques. LOCOS, once again, is an acronym derived from LOcal Oxidation of Silicon, with the underlined and capitalized letters forming the acronym. This technique has nothing to do with deposition of oxide. LOCOS uses a deep oxidation of the silicon substrate itself to provide a relatively thick oxide layer that is known in the art as a Field OXide or "FOX".

Shallow trench isolation techniques, on the other hand, involve formation of a vertical-walled trench, typically using reactive ion etching, followed by deposition of silicon dioxide, rather than oxidation of the silicon substrate material. As a result, shallow trench isolation features can be formed with far more control over lateral spread that occurs due to diffusion of oxygen in the oxide as it forms when the substrate itself is oxidized. This permits much greater packing density to be achieved. It also provides a more

planar surface because the excess deposited oxide is removed using chemical-mechanical planarization techniques.

Applicant claims such a process in conjunction with other aspects of the invention. As noted above and in the last response, these techniques are not arbitrarily interchangeable.

Forbes '351 does not teach any form of shallow trench isolation, as recited in Applicant's claims and as understood by those of skill in the relevant arts, and instead teaches formation of isolation regions using a different conventional isolation technique known as LOCOS, albeit in an unusual form.

As a result, Forbes '351 fails to teach or disclose, or provide enabling disclosure for, or suggest or motivate, the invention as recited in any of Applicant's claims. Since Forbes '351 fails to meet any of the criteria for anticipation, Forbes '351 cannot possibly meet them simultaneously. Accordingly, the anticipation rejection of claims 1-7 and 51-73 are in error and should be withdrawn, and claims 1-7 and 51-73 should be allowed.

Unpatentability is a legal term of art. Simply stating a conclusion that "it would have been obvious" to combine teachings from references or to modify or augment teachings from a reference does not meet the standards for a rejection under 35 U.S.C. §103(a) as set forth in The Manual of Patent Examination Procedure at §706.02(j), entitled "Contents of a 35 U.S.C. 103 Rejection." As a result, the proposed combination does not and cannot provide the invention as recited in any of Applicant's claims and thus cannot render Applicant's claims unpatentable. This is described in more detail

below with reference to MPEP §2142, entitled "Legal Concept of Prima Facie Obviousness".

This MPEP section states that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. There is no motivation identified anywhere in the references to modify the references to attempt to arrive at the subject matter of Applicant's claims.

This MPEP section also states: "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest **all** the claim limitations."

As noted above, Forbes '351 does not provide any teaching, disclosure, suggestion or motivation for Applicant's affirmative recitations of forming a plurality of shallow isolation trenches or of isolation using STI. Thus, the third prong of the test cannot be met.

As a result, there cannot possibly be a reasonable expectation of success from modifying Forbes' '351 teachings to attempt to arrive at the subject matter as recited in any of Applicant's claims. The rejection fails all three prongs of the test set forth in the MPEP for forming a prima facie case of obviousness.

This MPEP section further states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." Since neither of these prongs of the test are met at all, such can hardly be found in the prior art.

Accordingly, the rejection of claims 52, 53 and 74 is plainly defective and should be withdrawn, and claims 52, 53 and 74 should be allowed.

Additionally, substituting the shallow trench isolation process taught by Applicant for the trench and oxidation technique of Forbes '351 renders the teachings of Forbes '351 unsuitable for their intended purpose. Forbes '351 teaches (col. 6, line 32 et seq.) formation of island-like areas 300 of silicon. Forbes '351 teaches that the three dimensional nature of this island, and the fact that the source region 48 of transistor 28 and the drain region 46 of transistor 26 are formed above the isolation oxide allow both of these structures to be contacted with a single contact 310 (col. 5, lines 43-46). In turn, this facilitates formation of a gain memory cell requiring only two lines for operation (col. 2, lines 51-54; col. 11, line 52 et seq.).

Substituting Applicant's shallow trench isolation for the isolation process developed by Forbes '351 renders the teachings of Forbes '351 unsuitable for their intended purpose. Such is improper, as is explained below in more detail with reference to MPEP §2143.01, entitled "Suggestion or Motivation to Modify the References".

This MPEP section states that "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE". This MPEP section further states that "If proposed modification would render the prior art invention being modified unsatisfactory

for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." As a result, the unpatentability rejection is improper and should be withdrawn, and claims 52, 53 and 74 should be allowed.

Accordingly, and for at least these reasons, the anticipation and unpatentability rejections of claims 1-7 and 51-74 are clearly in error and should be withdrawn, and claims 1-7 and 51-74 should be allowed.

Dependent claims 2-7, 51-53, 55-62, 64-66 and 68-74 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**".

In view of the foregoing, allowance of claims 1-7 and 51-84 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 04/1/2002 By: _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/388,857
Filing Date ..... September 1, 1999
Inventor ..... Luan C. Tran
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... L. Schillinger
Attorney's Docket No. MI22-878
Title: Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY
RESPONSE TO JULY 1, 2002 FINAL OFFICE ACTION
AMENDMENT TO ACCOMPANY CPA FILING

Underlines indicate additions and [brackets] indicate deletions.

In th Specification

The Abstract on p. 27 has been amended as shown follows:

ABSTRACT OF THE DISCLOSURE

Semiconductor processing methods of forming transistors, semiconductor processing methods of forming dynamic random access memory circuitry, and related integrated circuitry are described. In one embodiment, active areas are formed over a substrate, with one of the active areas having a width of less than one micron, and with some of the active areas having different widths. A gate line is formed over the active areas to provide transistors having different threshold voltages. [Preferably] In one embodiment, the transistors are provided with different threshold voltages without using a separate channel implant for the transistors. [In another embodiment, a plurality of shallow trench isolation regions are formed within a substrate and define a plurality of active areas having widths at least some of which being no greater than about one micron, with some of the widths preferably being different. A gate line is formed over the respective active areas to provide individual transistors, with the transistors corresponding to the active areas having the different widths having different threshold voltages. In another embodiment, two field effect transistors are fabricated having different threshold voltages without using a separate channel implant for one of the transistors versus the other.]

In the Claims

Claims 75-84 have been added.

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